EENG 284

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Digital Design Lab

Lab 4

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The Guessing Game

Lab Solutions

# LFSR Module:

Verilog code for the body of the lfsr module (courier 8-point font single spaced).

module lfsr(inputSeed, outputRand);

input wire [3:0] inputSeed;

output wire [3:0] outputRand;

assign outputRand[0] = inputSeed[0] ^ inputSeed[2];

assign outputRand[1] = inputSeed[0];

assign outputRand[2] = inputSeed[1];

assign outputRand[3] = inputSeed[2];

endmodule

Table 2: The first iteration of the LFSR shown in Figure 8 when started at decimal 14.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| O3 | O2 | O1 | O0 | decimal |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 0 | 0 | 4 |

Testbench



**High Low Module:**

Verilog code for the body of the hiLow module (courier 8-point font single spaced).

module hiLow(seedSwitch, playSwitch, guessSwitch, randBut, hiLowBut, randSeg, greenLEDs, hiLowSeg);

input wire [3:0] seedSwitch, guessSwitch;

input wire [1:0] playSwitch;

input wire randBut, hiLowBut;

output wire [6:0] randSeg;

output reg [6:0] hiLowSeg;

output reg [3:0] greenLEDs;

wire [3:0] randNum;

wire [6:0] randHex;

wire randGTguess, randEQguess, randLTguess;

lfsr randomizer(seedSwitch, randNum);

hexToSevenSeg RandHex27 (randNum, randHex);

genericMux2x1 #(7) disp(7'b1111111, randHex, randBut, randSeg);

always @(\*)

case (playSwitch)

2'b00: greenLEDs = 4'b1111;

2'b01: greenLEDs = 4'b0111;

2'b10: greenLEDs = 4'b0011;

2'b11: greenLEDs = 4'b0001;

endcase

genericComparator #(4) randVsGuess(randNum, guessSwitch, randGTguess,randEQguess, randLTguess);

always @(\*)

case ({hiLowBut, randGTguess, randEQguess, randLTguess})

4'b0001: hiLowSeg = 7'b0001001; // rand < guess High

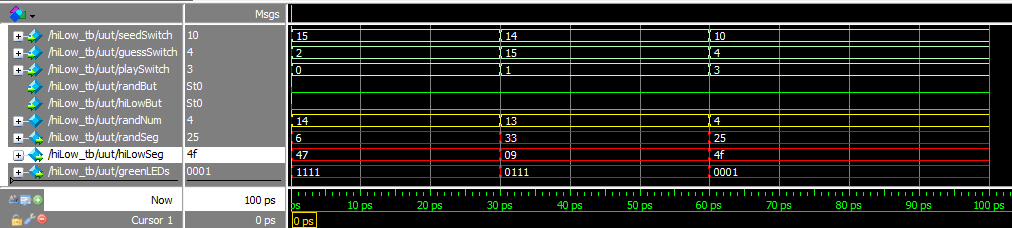
4'b0010: hiLowSeg = 7'b1001111; // rand = guess Win

4'b0100: hiLowSeg = 7'b1000111; // rand > guess Low

default: hiLowSeg = 7'b1111111;

endcase

endmodule



# Pin Assignment:

|  |  |  |
| --- | --- | --- |
| Segment | randSeg | hiLowSeg |
| seg[6] | PIN\_AC22 | PIN\_Y18 |
| seg[5] | PIN\_AC23 | PIN\_Y19 |
| seg[4] | PIN\_AC24 | PIN\_Y20 |
| seg[3] | PIN\_AA22 | PIN\_W18 |
| seg[2] | PIN\_AA23 | PIN\_V17 |
| seg[1] | PIN\_Y23 | PIN\_V18 |
| seg[0] | PIN\_Y24 | PIN\_V19 |

|  |  |  |  |
| --- | --- | --- | --- |
|  | seedSwitch | playSwitch | guessSwitch |
| slide[3] | PIN\_AE19 | N/A | PIN\_AC8 |
| slide[2] | PIN\_Y11 | N/A | PIN\_AD13 |
| slide[1] | PIN\_AC10 | PIN\_AB10 | PIN\_AE10 |
| slide[0] | PIN\_V10 | PIN\_W11 | PIN\_AC9 |

|  |  |  |
| --- | --- | --- |
| randBut | Key[3] | PIN\_Y16 |
| hiLowBut | Key[0] | PIN\_P11 |

|  |  |  |  |
| --- | --- | --- | --- |
| G[3] | G[2] | G[1] | G[0] |
| PIN\_E9 | PIN\_D8 | PIN\_K6 | PIN\_L7 |